Refine Search

Search Results -

Terms	Documents
L3 same (ram or dram or eprom or rom)	18

Database: US Pre-Grant Publication Full-Text Database; US Patents Full-Text Database; US OCR Full-Text Database; EPO Abstracts Database; JPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L8

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Monday, January 03, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L8	L3 same (ram or dram or eprom or rom)	18	L8
L7	L6 same memory	12	L7
L6	L5 same circuit	94	L6
L5	L2 same scrambl$	223	L5
L4	L3 same l2	6	L4
L3	scrambling adj1 circuit	418	L3
L2	constituted	664263	L2
DB=USPT; PLUR=YES; OP=OR			
L1	5850452[pn]	1	L1

END OF SEARCH HISTORY

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#

Generate Collection Print

L8: Entry 4 of 18 File: USPT May 14, 2002

DOCUMENT-IDENTIFIER: US 6389525 B1
TITLE: Pattern generator for a packet-based memory tester

Detailed Description Text (15):
To provide for conventional X and Y address scrambling, respective X and Y address scrambling circuits 146 and 148 are disposed between the pattern generator input and output multiplexer arrays 60 and 166. The scrambling circuits include respective 256K X and Y scramble RAMS 150 and 152 that act as lookup tables between the physical and logical X and Y addresses. The outputs of the scramble RAMs connect to respective selectors 154 and 156 that distribute the scrambled signals along respective X and Y scrambled address busses 158 and 160. Respective bypass connections 162 and 164 couple the unscrambled X and Y address signals to the selectors 154 and 156.

Previous Doc Next Doc Go to Doc#

First Hit Previous Doc Next Doc Go to Doc#

End of Result Set

Generate Collection Print

L7: Entry 12 of 12 File: JPAB Jan 22, 1991

PUB-NO: JP403014147A
DOCUMENT-IDENTIFIER: JP 03014147 A
TITLE: PROGRAM ENCIPHERING CIRCUIT

PUBN-DATE: January 22, 1991

INVENTOR-INFORMATION:
NAME COUNTRY
MAEDA, TOKUNORI

ASSIGNEE-INFORMATION:
NAME COUNTRY
FUJITSU LTD

APPL-NO: JP01150053
APPL-DATE: June 13, 1989

INT-CL (IPC): G06F 12/14; G06F 9/06; G09C 1/00

ABSTRACT:

PURPOSE: To simply perform various encipherments by providing an address scramble circuit, a semiconductor memory part and a data scramble circuit, containing in a chip or providing externally the semiconductor memory part, and containing the address scramble circuit and the data scramble circuit in the chip.

CONSTITUTION: An address scramble circuit 15 and a scramble circuit 16 of read-out data are constituted of a connection against a wiring. As for a program and data stored in a semiconductor memory part 12, its store position and contents are enciphered (scrambled), and when a program counter 11 is incremented by '0', 1, 2,..., the semiconductor memory part 12 is read out by an address which scrambles it, and when the read-out data is scrambled, normal data is obtained. In such a way, it is unnecessary to add a semiconductor circuit, etc., and by scrambling both the program and the data, various encipherments are performed simply.

Previous Doc Next Doc Go to Doc#

L8: Entry 13 of 18 File: USPT Jul 25, 1989

DOCUMENT-IDENTIFIER: US 4852101 A
TITLE: Apparatus for recording and/or reproducing optical cards

Detailed Description Text (30):
It is noted that the C.sub.2 -encoder 112, scrambling circuit 113, C.sub.1 -encoder 114 and scrambling circuit 115 in FIG. 10 are configurated in reality by RAM units (random access memory units), 121, 122 and a ROM unit (read only memory unit) 123 as shown in FIG. 11. That is, the C.sub.2 (20, 16) or C.sub.1 (24, 20) error check coding is implemented on the block-by-block basis for data supplied to and stored in the RAM 121 from the input terminal 124, so that checking words are added to the data. This error correction code processing is carried out in, for example, a digital signal processor, not shown. A counter 126 activated for counting responsive to clock signals from a clock input terminal 125 outputs read address signals for the RAM 121 and ROM 123. The check word data of the error check code and the data read from the RAM 121 responsive to these address signals are transmitted to the next stage scrambling RAM 122. Data writing into the RAM 122 is controlled responsive to the address data sequentially read from ROM 123 by the address signals supplied from the counter 126, in such a manner that the input data are sequentially written into the addresses in accordance with the scramble operation as shown in FIGS. 8 or 9. In other words, it is possible to regard FIGS. 8 or 9 as a memory map of the scramble processing RAM 122. Suppose that a RAM 122 having a memory capacity of a plurality of, such as 50, blocks, with each block consisting of 20 words, is used as the RAM for implementing the scramble operation shown in FIG. 8. If a data of the word W.sub.0,n is inputted, this is written into the address (block number n; word number 0) in the RAM 122; similarly, if a data of the word W.sub.1,n is inputted, this is written into an address (block number n+1; word number 2) and so on. The succeeding words are written in addresses in accordance with FIG. 8. Next, when read out, data of each word W'.sub.0,n to W'.sub.19,n for the n-th block of the word numbers 0 to 19 are read sequentially so that data to which the first scramble processing is implemented as explained with reference to FIG. 8 can be outputted from the output terminal 127. The second scramble operation can be implemented similarly. Further, it is possible to write data into the scramble processing RAM in the order of addresses and to read the data by controlling the addresses according to the scramble processing.

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#

Generate Collection Print

L4: Entry 3 of 6 File: USPT Jul 27, 1993

DOCUMENT-IDENTIFIER: US 5231667 A
TITLE: Scrambling/descrambling circuit

CLAIMS:

3. A scrambling circuit according to claim 1, wherein said scrambling circuit is constituted at least by a CMOS arrangement in LSI format.

Previous Doc Next Doc Go to Doc#

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#
Generate Collection Print

L4: Entry 3 of 6 File: USPT Jul 27, 1993

DOCUMENT-IDENTIFIER: US 5231667 A
TITLE: Scrambling/descrambling circuit

CLAIMS:

3. A scrambling circuit according to claim 1, wherein said scrambling circuit is constituted at least by a CMOS arrangement in LSI format.

Previous Doc Next Doc Go to Doc#

First Hit Previous Doc Next Doc Go to Doc#

Generate Collection Print

L4: Entry 5 of 6 File: JPAB Oct 29, 1993

DOCUMENT-IDENTIFIER: JP 05284153 A
TITLE: SCRAMBLE SIGNAL MULTIPLEXING SYSTEM

Abstract Text (2):
CONSTITUTION: The self-synchronizing scrambling circuit is constituted of five D-type FFs 101-A to 101-E and two exclusive OR circuits 101F and 101G. The output of the circuit 101-G is connected to the circuit 101-F and exclusively ORed with an input signal 1. The output of the circuit 101-F is inputted to the input D of the FF 101-A and outputted to the poststage as an output signal 2. An OR 101-H stops a clock signal to operate FFs by a scramble control signal 14 to be generated at a time base signal generating circuit 102 and stops the operation of D-type FFs. Thus, the action of the self-synchronizing scrambling circuit is stopped and the continuity of the scrambling signals to be generated is not lost by stopping the clock.

Previous Doc Next Doc Go to Doc#

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#

Generate Collection Print

L7: Entry 3 of 12 File: USPT Mar 23, 1999

DOCUMENT-IDENTIFIER: US 5887061 A
TITLE: Compression coding device with scrambling function and expansion reproducing device with descrambling function

Detailed Description Text (70):
The decoder 404 includes a memory circuit 404a for descrambling the scrambled image data received from the multiplexer 402. In the illustrative embodiment, the memory circuit 404a is implemented as a DRAM having a capacity great enough to store two frames of data Y, Cb and Cr. The capacity of the memory circuit 404a may be great enough to store three or more frames, if desired. A frame memory for storing the data Y, Cb and Cr is constituted by a first and a second frame memory. The coded data Y, Cb and Cr sequentially fed from the demultiplexer 402 in this order are sequentially repeatedly written to the first and second frame memories in this order. In this embodiment, while the data are written to the first frame memory, the data are read out of the second frame memory; while the data are written to the second frame memory, the data are read out of the first frame memory. The writing and reading of data out of such frame memories are controlled by a control signal fed from the controller 428 via a control line 512.

Previous Doc Next Doc Go to Doc#